AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1. (currently amended) A system for extending a signal path of a host bus comprising:

a first repeater portion connected to a first segment of the host bus;

a second repeater portion connected to a second, non-hierarchical segment of the host bus remote from the first portion of the host bus, where the first and second portions of the repeater are connected by a serial link.

2. (original) The system according to claim 1, wherein the serial link is chosen from one of the following: LVDS, Gigabit Ethernet, InfiniBand, IEEE1394, RF Wireless, Infrared Wireless, or any combination of these.

3. (original) The system according to claim 2, wherein the host bus is a PCI bus.

4. (original) The system according to claim 2, wherein the host bus is an LPC (Low Pin Count) bus as defined by Intel 1997.

5. (original) The system according to claim **1**, wherein at least one of the repeater portions further comprise:

an interface to the host bus segment;

a transaction queue with a data buffer connected to the interface;

a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

6. (original) The system according to claim **3**, wherein at least one of the repeater portions further comprise:

an interface to the host bus segment;

a transaction queue with a data buffer connected to the interface;

a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

7. (original) The system according to claim **2**, wherein at least one of the repeater portions further comprise:

an interface to the host bus segment;

a transaction queue with a data buffer connected to the interface;

a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

8. (original) The system according to claim **5**, further comprising a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link.

9. (original) The system according to claim **6**, further comprising a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link.

10. (original) The system according to claim **7**, further comprising a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link.

Claims 11-14 (canceled).